

<b>Notice of References Cited</b>	Application/Control No. 10/038,311	Applicant(s)/Patent Under Reexamination RICH ET AL.	
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**U.S. PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6,817,000	11-2004	Rich et al.	716/6
	B	US-2003/0125918 A1	07-2003	Rich et al.	703/14
	C	US-			
	D	US-			
	E	US-			
	F	US-			
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

**FOREIGN PATENT DOCUMENTS**

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE Standard 1497-2001. "IEEE Standard for Standard Delay Format (SDF) for the Electronic Design Process." Approved Dec.5, 2001.
	V	Open Verilog International . "Standard Delay Format Specification Version 2.1". February 1994.
	W	Open Verilog International . "Standard Delay Format Specification Version 3.0". May 1995.
	X	IEEE DASC Standard Delay Format (SDF). Last modified Dec. 17, 2001. Printed from <a href="http://www.eda.org/sdf/">http://www.eda.org/sdf/</a>

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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	N					
	O					
	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Fleischmann, J. et al. "OLIVIA: Object Oriented Logic Simulation Implementing the VITAL Standard." Proc. Seventh Great Lakes Symposium on VLSI (1997). March 1997. pp.51-56.
	V	Krolikoski, S.J. "Standardizing ASIC Libraries in VHDL Using VITAL: a Tutorial." Proc. of IEEE 1995 CUsom Integrated Circuits Conf., May 1-4, 1995. pp.603-610.
	W	Balaji, E. et al. "Modeling ASIC Memories in VHDL." Proc. of EURO-DAC '96. Sept. 16-20, 1996. pp.502-508.
	X	IEEE Std. 1076.4-2000. IEEE Standard for VITAL ASIC Modeling Specification. Approved Sept. 21, 2000. pp.1-14.

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
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	P					
	Q					
	R					
	S					
	T					

**NON-PATENT DOCUMENTS**

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	IEEE Std. 1076.4-1995. IEEE Standard for VITAL ASIC Modeling Specification. Approved Dec.12, 1995.
	V	
	W	
	X	

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